REMARKS

Claims 1-11 and 21-28 are all the claims pending in the application. Claims 1-11 stand rejected on prior art grounds. Claims 12-20 have been canceled without prejudice or disclaimer. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-2, 4-7 and 9-11 stand rejected under 35 U.S.C. §102(e) as being anticipated by Sugii et al., (U.S. Publication No. 2004/0108559 A1), hereinafter referred to as "Sugii". Claims 3 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sugii, in view of Wu et al. (U.S. Patent No. 6,770,516), hereinafter referred to as "Wu". Applicants respectfully traverse these rejections based on the following discussion.

Sugii teaches the possibility of avoiding deterioration in short-channel characteristics, caused by a silicon germanium layer coming into contact with the channel of a strained SOI transistor. Further, it is possible to fabricate a double-gate type of strained SOI transistor or to implement mixedly mounting the strained SOI transistor and a conventional silicon or SOI transistor on the same wafer. According to the invention, for example, a strained silicon layer is grown on a strain-relaxed silicon germanium layer, and subsequently, portions of the silicon germanium layer are removed, thereby constituting a channel layer in the strained silicon layer.

Wu teaches a method of forming a FINFET CMOS device structure featuring an N channel device and a P channel device formed in the same SOI layer, has been developed. The method features formation of two parallel SOI fin type structures, followed by gate insulator growth on the sides of the SOI fin type structures, and definition of a conductive gate structure formed traversing the SOI fin type structures while interfacing the gate insulator layer. A doped

insulator layer of a first conductivity type is formed on the exposed top surfaces of a first SOI fin type shape, while a second doped insulator layer of a second conductivity type is formed on the exposed top surfaces of the second SOI fin type shape. An anneal procedure results creation of a source/drain region of a first conductivity type in portions of the first SOI fin type shape underlying the first doped insulator layer, and creation of a source/drain region of a second conductivity type in portions of the second SOI fin type shape underlying the second doped insulator layer. Selective deposition of tungsten on exposed top surface of the source/drain regions is then employed to decrease source/drain resistance.

The claimed invention, as provided in amended independent claims 1 and 6 and newly added independent claim 21 include features, which are patentably distinguishable from the prior art references of record. Specifically, claims 1 and 6 include, in part, "wherein an upper surface of a gate region of said FET is planar to an upper surface of a gate region of said FinFET." Similarly, claim 21 includes, in part, "wherein said upper surface of said FinFET gate region and said upper surface of said FET gate region are at a same level."

Clearly these features are not taught or suggested in the prior art of record. First, the Office Action incorrectly describes the structure in Sugii (Figure 49) as a FinFET and one planar device. Those skilled in the art would readily recognize that this device is, in fact, two planar devices. For example, Wu illustrates and describes a FinFET device. See for example, Figure 11B in Wu. Conversely, in Figure 49 of Sugii, the device on the left is a planar FET gate on a strained silicon layer on oxide on insulating film on a substrate. The device on the right is a standard planar FET device on a substrate. While paragraph [0091] (page 5) of Sugii discuses FinFET devices, there is no teaching that such a device could be incorporated into a single structure with a standard FET device whereby the gate regions on each device are planar (i.e., the

respective upper gate surfaces are at the same upper level).

Furthermore, the process described to build the standard structure in Figure 49 of Sugii is significantly different than the process used to build the FinFETs in the Sugii application. As such, if Sugii were to utilize his technique of building FinFETs on the same structure as a standard FET device, then it would result in significant height differences between the FET gate and the FinFET gate. Those skilled in the art would readily acknowledge that the two processes (i.e., process of building FinFETs and process of building standard FETs) are significantly different from one another and are not easily combined until the Applicants were able to successfully do so. Again, if the processes in the Sugii application were highly modified so that they could be integrated, then the resulting FinFET gate would not be planar with the FET gate region as is provided in Applicants' independent claims 1, 6, and newly added independent claim 21.

Hence, Sugii combines two standard planar FET devices and not a FinFET device and a standard FET device as erroneously concluded in the Office Action. Conversely, the claimed invention provides a planar FET device in the substrate and a FinFET on a SOI substrate. Moreover, even if Sugii were to be combined with Wu, they would still fail to teach the elements of Applicants' claimed invention.

In view of the foregoing, the Applicants respectfully submit that the cited prior art, either alone or in combination with one another, do not teach or suggest the features defined by independent claims 1, 6, and 21 and as such, claims 1, 6, and 21 are patentable over Sugii and/or Sugii in combination with Wu. Further, dependent claims 2-5, 7-1, and 22-28 are similarly patentable over Sugii and/or Sugii in combination with Wu, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional

features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

While the claims have been amended, they have not been amended in an effort to overcome the prior art rejections. Rather, the amendments are made to more clearly define the claimed subject matter. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-11 and 21-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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